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FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

CD4027BC
Dual J-K Master/Slave Flip-Flop with Set and Reset

General Description

The CD4027BC dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent J, K, set, reset, and clock inputs and buffered Q and $\overline{Q}$ outputs. These flip-flops are edge sensitive to the clock input and change state on the positive-going transition of the clock pulses. Set or reset is independent of the clock and is accomplished by a high level on the respective input.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- Low power: 50 nW (typ.)
- Medium speed operation: 12 MHz (typ.) with 10V supply

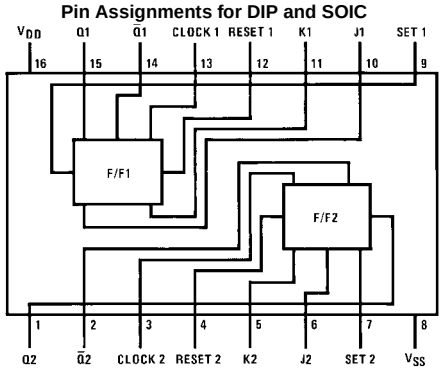
Ordering Code:

Order Number	Package Number	Package Description
CD4027BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD4027BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP and SOIC



Top View

Truth Table

Inputs t_{n-1} (Note 1)						Outputs t_n (Note 2)	
CL (Note 3)	J	K	S	R	Q	Q	$\overline{Q}$
⌐‾	I	X	O	O	O	I	O
⌐‾	X	O	O	O	I	I	O
⌐‾	O	X	O	O	O	O	I
⌐‾	X	I	O	O	I	O	I
‾⌙	X	X	O	O	X		(No Change)
X	X	X	I	O	X	I	O
X	X	X	O	I	X	O	I
X	X	X	I	I	X	I	I

I = HIGH Level
O = LOW Level
X = Don't Care
⌐‾ = LOW-to-HIGH
‾⌙ = HIGH-to-LOW

Note 1: t_{n-1} refers to the time interval prior to the positive clock pulse transition

Note 2: t_n refers to the time intervals after the positive clock pulse transition

Note 3: Level Change

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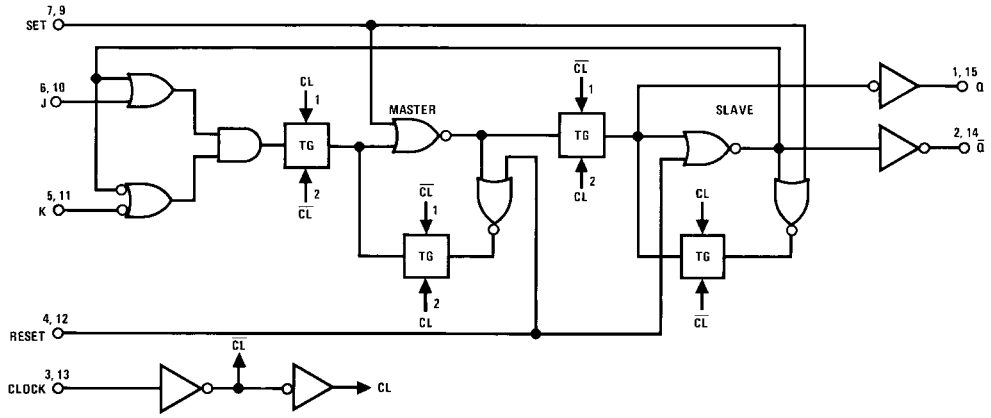
Logic Diagram



Absolute Maximum Ratings (Note 4)

(Note 5)

DC Supply Voltage (V_{DD})	−0.5 V_{DC} to +18 V_{DC}
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 5)

DC Supply Voltage (V_{DD})	3V to 15 V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	−40°C to +85°C

Note 4: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 5: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 6)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		4			4		30	µA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		8			8		60	µA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		16			16		120	µA
V_{OL}	LOW Level	$\|I_O\|$ < 1 µA								
	Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level	$\|I_O\|$ < 1 µA								
	Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	LOW Level	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
	Input Voltage	V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	HIGH Level	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
	Input Voltage	V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	LOW Level Output	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
	Current (Note 7)	V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	HIGH Level Output	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
	Current (Note 7)	V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	µA

Note 6: V_{SS} = 0V unless otherwise specified.

Note 7: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 8)

$T_A = 25°C$, $C_L = 50$ pF, $t_{rCL} = t_{fCL} = 20$ ns, unless otherwise specified

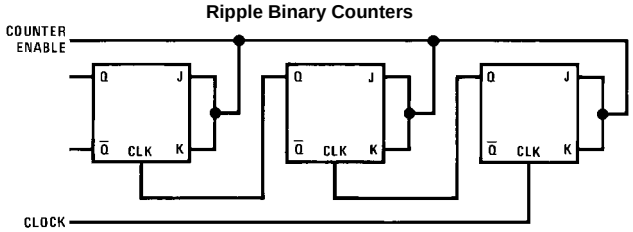
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		200	400	ns
	from Clock to Q or $\overline{Q}$	$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		65	130	ns
t_{PHL} or t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		170	340	ns
	from Set to $\overline{Q}$ or Reset to Q	$V_{DD} = 10V$		70	140	ns
		$V_{DD} = 15V$		55	110	ns
t_{PHL} or t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		110	220	ns
	from Set to Q or	$V_{DD} = 10V$		50	100	ns
	Reset to $\overline{Q}$	$V_{DD} = 15V$		40	80	ns
t_S	Minimum Data Setup Time	$V_{DD} = 5V$		135	270	ns
		$V_{DD} = 10V$		55	110	ns
		$V_{DD} = 15V$		45	90	ns
t_{THL} or t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	2.5	5		MHz
	(Toggle Mode)	$V_{DD} = 10V$	6.2	12.5		MHz
		$V_{DD} = 15V$	7.6	15.5		MHz
t_{rCL} or t_{fCL}	Maximum Clock Rise	$V_{DD} = 5V$	15			µs
	and Fall Time	$V_{DD} = 10V$	10			µs
		$V_{DD} = 15V$	5			µs
t_W	Minimum Clock Pulse	$V_{DD} = 5V$		100	200	ns
	Width ($t_{WH} = t_{WL}$)	$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		32	65	ns
t_{WH}	Minimum Set and	$V_{DD} = 5V$		80	160	ns
	Reset Pulse Width	$V_{DD} = 10V$		30	60	ns
		$V_{DD} = 15V$		25	50	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacity	Per Flip-Flop		35		pF
		(Note 9)				

Note 8: AC Parameters are guaranteed by DC correlated testing.

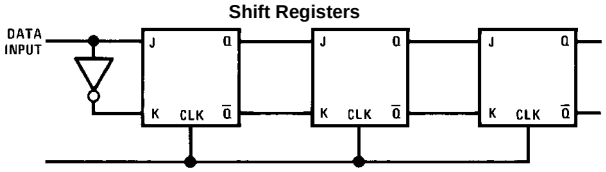
Note 9: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 74C Family Characteristics application note, AN-90.

Typical Applications

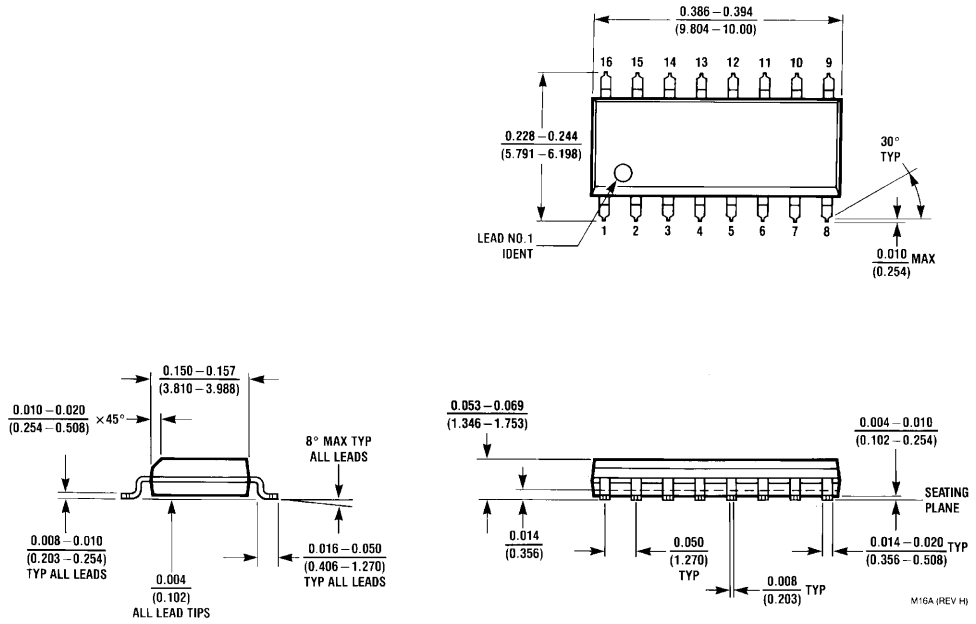
Ripple Binary Counters



Shift Registers

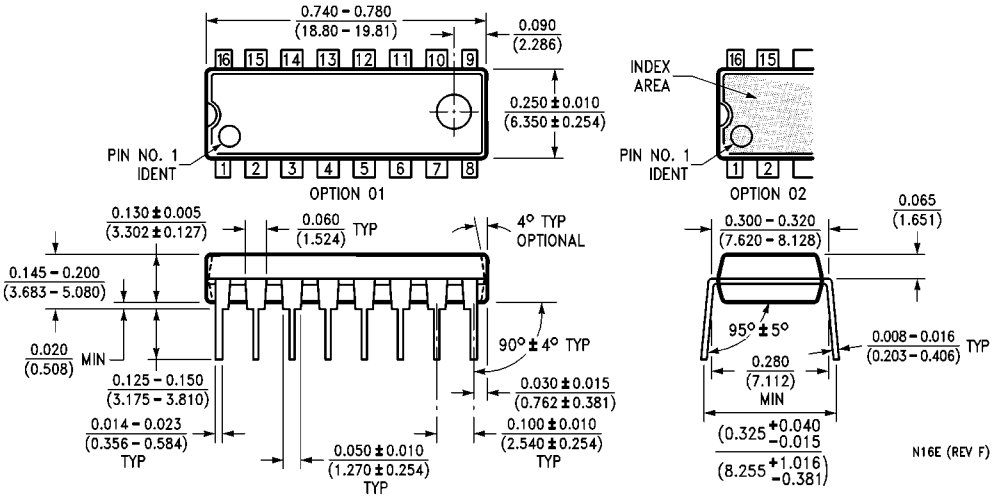


Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow Body
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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